of ordinary skill in the art will recognize that the bias voltages can readily be optimized for device-size scaling and different doping levels.

In the Claims:

Kindly amend the claims as follows:

1. (Original) A transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

a p-type region disposed over said n-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a control gate disposed above and insulated from said channel;

said substrate, said n-type region and said p-type region each biased such that said p-type region is fully depleted.

2. (Original) The transistor of claim 1 wherein said n-type region is a well region.

3. (Original) The transistor of claim 1 wherein said p-type region is a well region.

4. (Currently Amended) The transistor of claim ~~2~~ 3 wherein said n-type region is a well region.

5. (Original) The transistor of claim 1 wherein said n-type region is a buried layer.

6. (Original) The transistor of claim 5 wherein said n-type region is a buried layer laid out in a grid formation.

7. (Original) The transistor of claim 1 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said n-type region.

8. (Original) A transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

9. (Original) The transistor of claim 8 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

10. (Original) A floating-gate transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

a p-type region disposed over said n-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a floating gate disposed above and insulated from said channel; and

said substrate, said n-type region and said p-type region each biased such that said p-type region is fully depleted.

11. (Original) The floating-gate transistor of claim 10 wherein said n-type region is a well region.

12. (Original) The floating-gate transistor of claim 10 wherein said p-type region is a well region.

13. (Currently Amended) The floating-gate transistor of claim ~~11~~ 12 wherein said n-type region is a well region.

14. (Original) The floating-gate transistor of claim 10 wherein said n-type region is a buried layer.

15. (Original) The floating-gate transistor of claim 14 wherein said n-type region is a buried layer laid out in a grid formation.

16. (Original) The floating gate transistor of claim 10 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said n-type region;

17. (Original) A floating-gate transistor for an integrated circuit comprising:

a p-type substrate;

an n-type region disposed over said p-type substrate;

n-type buried layers disposed at about a boundary between said substrate and said n-type region, said buried layers doped to a higher level than said n-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate; and

said substrate, said n-type region and said n-type buried layers each biased such that said n-type region is fully depleted.

18. (Currently Amended) The floating-gate transistor of claim ~~16~~ 17 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

19. (Original) A transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

an n-type region disposed over said p-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said p-type region and said n-type region each biased such that said n-type region is fully depleted.

20. (Original) The transistor of claim 19 wherein said p-type region is a well region.

21. (Original) The transistor of claim 19 wherein said n-type region is a well region.

22. (Currently Amended) The transistor of claim ~~20~~ 21 wherein said p-type region is a well region.

23. (Original) The transistor of claim 19 wherein said p-type region is a buried layer.

24. (Original) The transistor of claim 23 wherein said p-type region is a buried layer laid out in a grid formation.

25. (Original) The transistor of claim 19 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said p-type region.

26. (Original) A transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a control gate disposed above and insulated from said channel; and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

27. (Original) The transistor of claim 26 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.

28. (Original) A floating-gate transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

an n-type region disposed over said p-type region;

spaced apart p-type source and drain regions disposed in said n-type region forming a channel therein;

a floating gate disposed above and insulated from said channel; and

said substrate, said p-type region and said n-type region each biased such that said n-type region is fully depleted.

29. (Original) The floating-gate transistor of claim 28 wherein said p-type region is a well region.

30. (Original) The floating-gate transistor of claim 28 wherein said n-type region is a well region.

31. (Currently Amended) The floating-gate transistor of claim ~~29–~~30 wherein said p-type region is a well region.

32. (Original) The floating-gate transistor of claim 28 wherein said p-type region is a buried layer.

33. (Original) The floating-gate transistor of claim 32 wherein said p-type region is a buried layer laid out in a grid formation.

34. (Original) The floating gate transistor of claim 28 further including an isolation trench disposed in said n-type region and surrounding said source and drain regions, said isolation trench extending down into said p-type region.

35. (Original) A floating-gate transistor for an integrated circuit comprising:

an n-type substrate;

a p-type region disposed over said n-type substrate;

p-type buried layers disposed at about a boundary between said substrate and said p-type region, said buried layers doped to a higher level than said p-type region;

spaced apart n-type source and drain regions disposed in said p-type region forming a channel therein;

a floating gate disposed above and insulated from said channel;

a control gate disposed above and insulated from said floating gate; and

said substrate, said p-type region and said p-type buried layers each biased such that said p-type region is fully depleted.

36. (Original) The floating-gate transistor of claim 35 further including an isolation trench disposed in said p-type region and surrounding said source and drain regions, said isolation trench extending down into said substrate.